

Measuring IC Project Development Productivity

White Paper

Developed by
Numetrics Management Systems, Inc.
20863 Stevens Creek Blvd, Suite 510 Cupertino, CA 95014
Tel: (408) 351 5800 Fax: (408) 351 5850
Email: info@numetrics.com
Web site: www.numetrics.com

I. Introduction

Maximizing productivity for IC product development has become critical for semiconductor and electronics systems companies. The capability to rapidly develop complex SoC's—and, increasingly, software and IP blocks—is a tremendous competitive advantage, and high development productivity is pivotal. Equally important is a reliable calibration of the organization's productivity, not just because it's a prerequisite for establishing a baseline and monitoring improvement, but also because it is essential for estimating the engineering resources needed to meet today's intensely competitive development schedules. Likewise, it is an indispensable for accurate capacity planning.

Furthermore, owning a fab no longer offers the competitive advantage it once did. The availability of manufacturing services from dedicated silicon foundries has leveled the playing field between semiconductor companies that have fabs and those that don't. Fabless chip houses have just as much access to leading-edge process technology as vertically integrated device manufacturers (IDMs). As a result, development capability is now the fundamental differentiator, which calls for top-notch development productivity, rapid development cycles and near perfect schedule predictability.

As semiconductor companies strengthen their development capabilities and incorporate more functionality into their products, systems companies must distinguish their high-end products from those built with semiconductor vendors' off-the-shelf chips. Therefore, to achieve competitive differentiation, they must design chips that are even more advanced than the commercial products from semiconductor companies. So for systems companies, too, the need to lead in development capability, and therefore to top the list in design productivity, has never been as important as it is today.

In sum, development capability has emerged as a key area of differentiation and competitive advantage among companies in the electronics industry. A prerequisite to improving development productivity is measuring it. That's one reason why leading-edge semiconductor development organizations are benchmarking and calibrating their IC development capability determinedly. They are leveraging these baseline measurements not only to establish reference points for productivity improvement, but also as a means to rigorously assess resource requirements on their next projects. Resource levels must reflect the design's complexity, the project's schedule constraints and maximum productivity achievable by the team. Only when these parameters align can the project finish on time and within budget.

II. Defining IC Product Development Productivity

The starting point for measuring development productivity is a clear definition. Numetrics recommends the standard industrial definition of productivity (P), which is the Output (that the development team produces) divided by the Labor Input to develop it—that is, the effort expended in producing that output. Therefore,

$$P = (\text{Output}) \div (\text{Labor [effort] expended to produce Output})$$

The resulting dimension of productivity is Output per unit of Labor Input.

Applying this definition to IC product development productivity immediately raises several important questions. First, what's the Output of a development team; that is, what does it produce? Second, what should be included in the Labor Input? In other words, what product development activities should be included? This requires a clear and consistent definition of the project's beginning and end milestones, because they determine when the labor clock starts and stops?

III. Labor Input

a. Dimension of Labor Input

Effort expended to produce a unit of output is the denominator of the productivity equation. To obtain effort expended, Numetrics uses the concept of an FTE (full-time equivalent worker). One FTE equals a person working full time for a full year. So an FTE is 52 person-weeks and is a measure of the staffing level equivalent to one person working full-time on a project. One FTE can be one person spending all their time on a project, or two people spending half their time on a project. In other words, if a person divides their time equally between two different projects during a specific time period, that person is counted as 0.5 FTE on each project; if on three projects, 0.33 FTE; and so on. Likewise, one person working 100 percent of their time on a project is one FTE. The use of person-weeks, or FTEs, provides a consistent, dependable, and relatively simple way to measure effort.

Although using person-hours instead of FTE is arguably more precise, this would require the exact number of hours expended by each person be captured consistently and accurately on each project; otherwise, the data can't be used to make fair and accurate comparisons, because even a small error or inconsistency could significantly alter the productivity calculation. But different organizations use different methods to collect effort data, which makes it impractical to capture that level of detail.

Through extensive experience, Numetrics has found that measuring effort in terms of FTE's is far more optimal than person-hours. It turns out that the *average* work-week of a development team member (averaged across the entire IC development cycle) in the semiconductor industry varies little from one company or organization to the next. That's because, over a long project, there's a natural upper limit to the number of hours a week a person can work. And there's always a lower limit, which is the number of hours officially designated as the company's workweek. As a result, for a long project, the variation in the number of hours an employee works averages out.

b. Project Start and End Milestones

The development cycle is defined as the period of time in which the development team produces its output. Under the Numetrics definition, the interval is from the start-of-concept phase (project start milestone) to release-to-volume production (project end milestone). Start-of-concept occurs at the point in time when a commitment is made to evaluate a specific product concept. This is when the "clock" starts. The definition takes into account the total cost of developing the IC, in terms of both time and effort, and it includes all personnel that expended effort on the project, including engineering, management, marketing, etc.

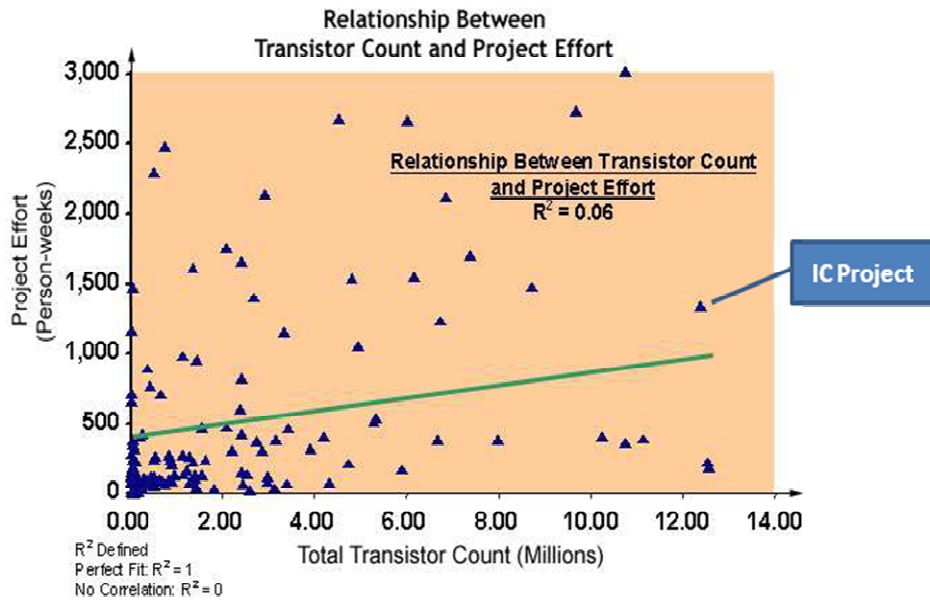
A development team's output takes the form of transistors and gates, but neither transistor count nor gate count accurately reflect differences in design complexity and therefore engineering effort from one chip to another. The industry abandoned transistor- and gate-count as measures of complexity years ago, with the integration of large memory blocks, RF circuits, analog and mixed-signal functions, processor cores and the widespread practice of design reuse.

As an example, consider that analog circuits are typically far more complex than digital circuits and, therefore, demand much more engineering effort to create. A 10-million transistor chip with 30% analog circuits typically requires much more development effort than a 10-million transistor chip that's purely digital logic. Similarly, within the digital domain, memory circuits require much less development effort than logic circuits, because they're generated automatically with memory compilers. Furthermore, many high-transistor-count designs require significantly less effort than many small designs.

In fact, there is little correlation between transistor count and the amount of effort expended on developing a chip. Each triangle in Figure 1 represents the measured transistor count and project effort of a real, completed IC development project. In other words, not all transistors are created with equal effort. So a productivity metric whose

dimensions are transistors per unit of labor input doesn't stand up as an accurate measure.

Figure 1:



With an R^2 value of 0.06, the data illustrates that there is very poor correlation between engineering effort expended on chip design and the total number of transistors in the design. As shown, many large designs require significantly less effort than many small designs. Likewise, many small designs require significantly more effort than many large designs. *Source: Numetrics*

Instead of using transistors or gates to quantify output, what's needed is mathematical model that rigorously quantifies the design difficulty associated with the chip's technical design characteristics and requirements. Such quantification would enable fair comparisons of complexity, or design difficulty, from one design to another, because the calculation would take into account the differences of each chip.

One way to model design difficulty is to quantify it in terms of average manpower required to design the chip. Under this scenario, the model would calculate the total amount of effort the average team in the semiconductor industry would normally expend to develop that particular chip (i.e. the manpower consumed from concept to release-to-production). Using this approach, the calculated effort operates as a proxy for design difficulty. For instance, if the calculated effort, which we can refer to as "Industry Norm Effort," for one chip is 20 FTE's and another is 10 FTE's, the former

would be exactly twice as complex as the latter, and the calculation reflects all of the attributes of each chip.

This is how Numetrics' project planning, risk analysis and benchmarking tools quantify the output of an IC development team and, therefore, IC design complexity. Calculating complexity in terms of the amount of effort typically required to design the chip yields an intuitive scale by which to measure and calibrate output. However, achieving high accuracy, which is determined by the model's predictive power – measured in terms of predicted effort vs. actual effort – demands that the model take into account all of the characteristics that have a material impact on project effort. That requires a large amount of empirically gathered data. Numetrics' model is calibrated with over 1,200 IC projects from nearly 40 semiconductor companies, including Intel, Texas Instruments, ST Microelectronics, Qualcomm, Samsung, Toshiba, Renesas, NXP, Infineon, Freescale, Sony, Matsushita, Fujitsu, Hewlett-Packard and many others. Model updates occur regularly using data extracted from new projects – data found to have a statistically significant impact on project effort.

With an objective, reliable way to quantify the output of a development team, engineering managers can not only measure productivity, they can also compare one chip's complexity to another, because output and complexity are one and the same. This is invaluable during the planning stage of a project, when resource planning and schedule estimation takes place.

V. Productivity – Ratio of Industry Norm Effort to Actual Effort Expended

Dividing a chip's Industry Norm Effort by the amount of effort the development team actually expended on the project (or is planning to spend on a new project) yields an accurate measure of productivity. In other words, if the effort calculated by the model is a calculation of the amount of effort the average team in the industry would expend on a particular chip design, then the ratio of the Industry Norm to the actual effort expended provides a measure of productivity:

$$\text{Productivity} = \frac{\text{Industry Norm Effort}}{\text{Actual Effort}}$$

A productivity value of 1.0 means that the particular team's productivity is exactly industry average.

A value of greater than 1.0, for example 1.5, would mean that the productivity of the team on that project was 50 percent higher than industry norm. Likewise, a value of less than 1.0, for example 0.7, means that the productivity of that team is 70 percent of industry norm.

When the effort in the denominator is the planned effort, as opposed to the actual effort, the calculation is the productivity that the team is assuming in its *project plan*. When applied in this fashion, the productivity calculation becomes a powerful tool for quantifying schedule risk. Here, the newly planned project's implied productivity can be compared to the actual productivity of finished projects. When the planned project's implied productivity is significantly greater than the historical productivity measured on finished projects, the schedule risk on the new project is high. That's because the new project is implicitly assuming a productivity that is well beyond what has been achieved in the past. Unless there is credible justification for such an assumption, it is very likely that the project will over-run its planned schedule. The exact probability of a schedule miss is easily calculated.

When comparing the productivity of one project to another, it is important to compare projects whose characteristics are similar. Projects that are similar in application, in design style, and in as many aspects as possible, should be grouped together when making productivity and complexity comparisons. To form an acceptable group of projects, one needs a sufficient number of similar projects, and that depends on having a large database of projects—the finer the granularity of the grouping and the larger the database size, the more reliable the comparisons.

The combination of Numetrics' patented complexity calculation engine and its industry database of more than 1,200 projects enables meaningful measurements of schedule risk and development team capability.

Summary

Measuring and improving the productivity of the IC development team has increased in importance for both semiconductor and systems companies. Organizations that measure their productivity have an inherent competitive advantage over firms that don't. First they are able to perform quantitative schedule risk assessments, enabling them to quickly identify project plans whose targets are not likely achievable. Second, their capacity planning process is accurate and reliable. Third, they can determine how their development capability stacks up against the industry. Lastly, it gives them a baseline for quantitatively monitoring development productivity improvement.

The key to measuring productivity is being able to fairly assess the output of the development team. One way to quantify the output is to develop a model that calculates Industry Norm Effort, which is the effort that would be expended on the particular IC design project by the average team in the industry. The Industry Norm Effort not only quantifies the output, it also accurately reflects the complexity, or design difficulty of that project. Underpinned by a database of more than 1,200 completed projects, Numetrics' IC design complexity calculation achieves this. The engine has been successively and continuously refined and is now in its eighth generation. First used by the Numetrics' consulting organization to benchmark industry clients, the engine has now been embedded in the firm's suite of resource planning tools. Balancing accuracy with ease of use, the engine and tools are being applied by semiconductor companies and IC development organizations throughout the industry as they endeavor to improve their product development competitiveness.