

# Complexity Calculation Engine

## Design Complexity

The IC Design Complexity Calculation Engine quantifies the complexity of designing a particular chip. The calculation is performed through extensive analysis of the chip's technical characteristics. The engine supports virtually any kind of semiconductor application, including communications, computing, multimedia, industrial and automotive, regardless of whether the project is a small analog-RF device or complex processor.

The models comprising the engine are regularly recalibrated to reflect changes in:

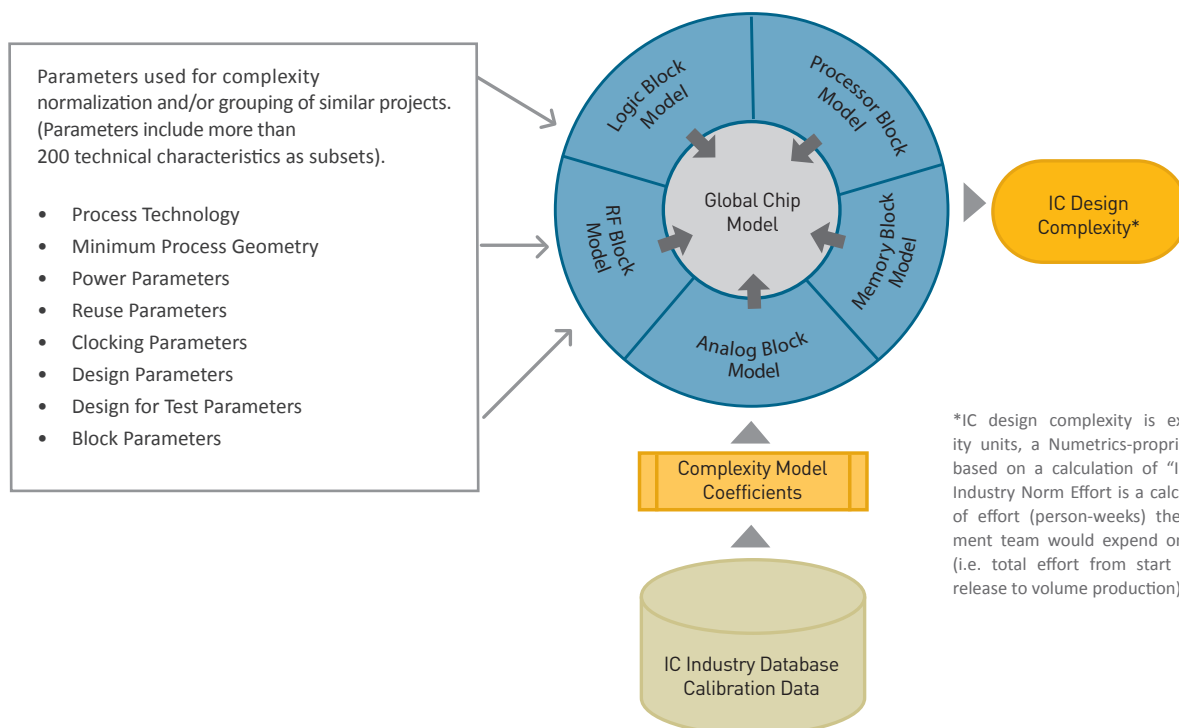
- IC design
- Technology
- Engineering skills
- Design methodology
- And more.

## Comprehensive, Targeted Inputs

To accurately and reliably quantify design complexity, Numetrics' calculation engine analyzes the target design's technical characteristics—those revealed through extensive data mining of its Industry Database to have a statistically significant impact on engineering effort. The Database is composed of more than 1,600 IC projects from nearly 75 semiconductor and electronics companies.

The engine's accuracy is the foundation for generating reliable project estimations—resource requirements, development cycle times and key performance indicators such as productivity and throughput.

Underpinning the engine is a model that calculates “industry-standard effort”—the amount of effort the average development team in the industry would spend on that design, from start-of-concept to release-to-volume production. The calculation of industry standard effort is the basis for reliably measuring complexity.



\*IC design complexity is expressed in complexity units, a Numetrics-proprietary metric which is based on a calculation of “Industry Norm Effort.” Industry Norm Effort is a calculation of the amount of effort (person-weeks) the average IC development team would expend on developing the chip (i.e. total effort from start of concept phase to release to volume production).

Initial complexity estimates are available with less than an hour of work via the engine's powerful Quickstart front-end. Typical accuracy is +/- 15 percent compared with the more detailed data entry option (which normally takes two to eight hours). With QuickStart, users enter a small but highly select subset of the design's technical characteristics—those shown statistically to have the greatest impact on project effort.

QuickStart enables users to generate estimates well before either the design is approved or engineering resources are assigned. The complexity calculation engine requires only high-level design information, such as the data available when RFQ (Request for Quote) alternatives are being explored. Further details of the design's technical description are successively and incrementally entered as they become available, including alternative scenarios of the chip's functionality and target implementation.

As implementation details become available, such as logic and circuit block parameters, users enter them into the engine to get an even more accurate calculation. Consistency of complexity calculations among different designs is ensured through simple, but rigorous data entry rules and policies.

### Empirically-calibrated Model = Real-world Accuracy

The engine analyzes each of the blocks comprising the chip. Block-level complexity analysis results are combined with the chip-level complexity model, where they are analyzed together to calculate the final design complexity value.

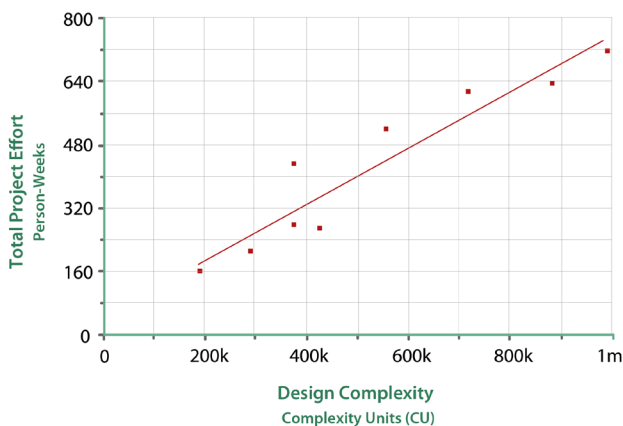
The complexity engine accurately calculates industry-standard effort because its underlying model is calibrated with data from actual, production-released IC projects – over 1,600. Thus, it is an empirically-calibrated model.

When users submit a chip description, the model naturally expects a realistic set of inputs and values – because its coefficients are derived from actual observations – as opposed to an impracticable, hypothetical combination. It is the set of real-world input values that enables the engine to reliably calculate industry-standard effort.

This is in contrast to a theoretical model, which often accepts unrealistic combinations of inputs and therefore generates theoretical outputs. A theoretical model says, for example, that adding layers of metallization to an IC, all else remaining constant, makes IC routing less complex because there is more area to route interconnect. In a theoretical environment this would be a correct outcome, but in the real world, all else rarely remains constant. Instead, metal layers, together with the complexity of the IC's technical specification, increase in *lockstep* – they are not independent of each other. Physical layout teams add layers only when no viable alternatives exist – because each layer adds manufacturing cost. For instance, if a layer of metal is added, other parameters change as well, such as transistor count, clock frequencies, die size, etc. A well-founded statistical model takes this into account. The advantage of an empirically-calibrated model is that it enables users to explore different complexity scenarios based on realistic combinations of inputs, not unrealistic, hypothetical sets.

This highly effective approach results in a very high correlation between the model's estimate of project complexity and the time required to complete the project in person weeks. For example, this is illustrated in the chart on the left showing the complexity/effort relationship for recent projects in the mobile audio category.

Total Project Effort vs. IC Design Complexity



**Note:** Total Project Effort includes all effort expended on the project, with the exception of effort spent on software development, which is treated separately by the complexity calculation engine.



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