

# NXP Wireless Development Team Confronts- Risks of Multi-site R&D



## In Brief...

### The Challenge

To develop a compact, single 2G/EDGE chip with a Multi-site R&D team and meet a very narrow market window.

### The Solution

IC Project Planner™ to provide accurate schedule estimates early in the chip planning process.

### The Impact

Went into project with a realistic schedule which was achieved with no schedule slip.

### The Value

Numetrics Tools enable a more constructive discussion between marketing, development and management people on realistic schedules.

Adrian Messmer is an IC Development Manager for NXP Semiconductors, headquartered in the Netherlands. His group of around 15 designers is part of a team that is responsible for creating chips used in 2G and 3G mobile phones.

Since joining NXP (previously Philips Semiconductors) in 1996, this seasoned veteran has been through countless chip design projects—each one presenting new challenges.

A recent project, sought to develop a compact, single 2G/EDGE chip with capabilities for video and a camera. With projected volumes in the millions and the market window narrow, the stakes were high -- the risks even higher.

Complicating development was the decision to utilize a new team of designers located in Shanghai, China. Messmer had no previous experience or track record working with the group, which was still ramping up. Managing such a remote team would not be easy.

*“Working with teams in southern France or Germany, we could get on a plane and be there in an hour,”* says Messmer. *“That wasn’t possible in this case.”* Even more critical, how would Messmer determine the resources needed to meet the deadline demanded by the marketing group? Guessing wrong could cause millions in investment and lost opportunities if the project fell too far behind and had to be terminated.

## The Solution

Messmer found the solution—IC Project Planner™ from Numetrics, which provides accurate, top-down<sup>1</sup> schedule estimates very early in the chip planning process. Planner combines Numetrics’ patented design complexity calculation engine with its project plan synthesis technology. The tool measures schedule risk and generates schedule and staffing estimates for chip development projects. It measures schedule risk by calculating the design’s complexity and then bench-

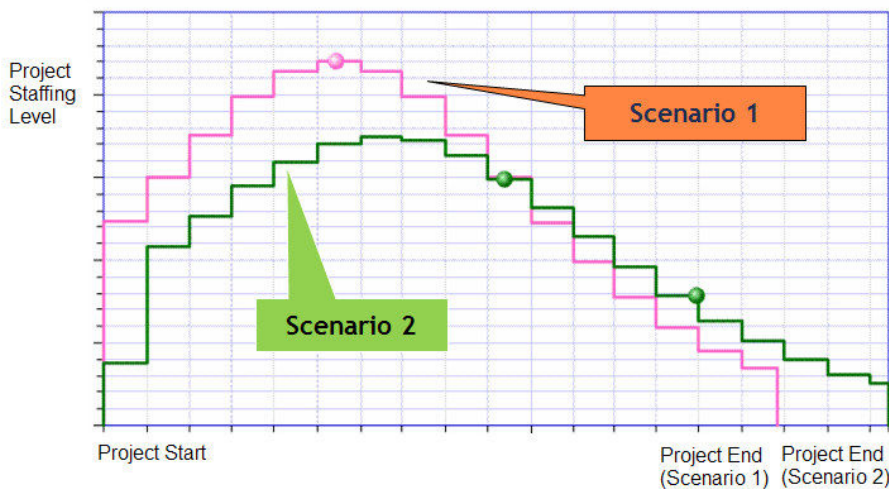
marking the project plan’s schedule and staffing assumptions against industry norms and past performance. Planner creates schedule estimates based on the chip’s complexity and the manager’s staffing plan. Conversely, it bases staffing estimates on chip complexity and schedule constraints the manager imposes, calculating required team size and the corresponding productivity requirement. In addition to generating estimates of cycle time and staffing, the tool enables

<sup>1</sup> In this context, “top-down” refers to Numetrics’ proprietary methodology for generating estimates. The methodology uses Numetrics’ patented IC design complexity calculation engine, which is calibrated using over 1,400 benchmarked IC projects from more than 100 semiconductor companies, to determine the precise complexity of the chip and then combines this with information about the team to generate accurate estimates of schedule and staffing level requirements.

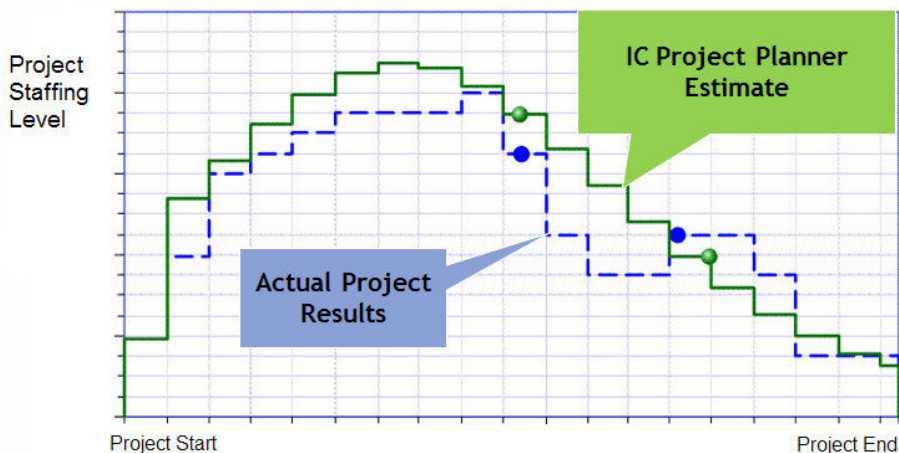
users to rapidly perform tradeoffs among the critical constraints on the project: schedule vs. staffing-level vs. chip complexity. In this way, the tool supports “what-if” project plan simulation.

Messmer first began using Numetrics in 2005. “Numetrics allows us to have a more constructive discussion between marketing people, development people, and management people about what is a realistic schedule,” says Messmer. “Overly aggressive IC development schedules are clearly identified. We use Planner during the planning stage for every project.”

The Development Manager applied Numetrics Planner to the early in the concept development phase. The Numetrics tool estimated the first tape out across a range of different staffing scenarios. For the scenario that Messmer selected, the Planner estimate proved accurate [See Figure 1]. Only a few weeks separated actual from what Planner estimated. “The difference was largely due to the uncertainty of how fast we could ramp up the team in Shanghai,” says Messmer. “The bottom line is we went into this project with a realistic schedule, which we achieved with no slip.” [See Figure 2]



**Figure 1**  
IC Project Planner Allows “What-if” Scenarios to Trade-off Resources with Schedule



**Figure 2**  
Estimated Completion using Numetrics Planner vs. Actual Completion Tracked Extremely Well

### Clear Visibility into the Execution Pipeline

Another Numetrics tool that Messmer leverages is the MultiProject Pipeliner™. Pipeliner reveals whether total resource demand from *multiple* IC development projects in the execution pipeline exceeds availability during the target time horizon—for each role (logic designers, verification engineers, analog designers, etc.).

Because it uses Numetrics' proprietary top-down methodology, Pipeliner alerts Messmer in the early stages of project planning as to whether enough staffing of each role is available to finish all projects on schedule. *"We use Pipeliner to provide management with a quarterly overview of IC projects in the pipe,"* says Messmer.

NXP and Adrian Messmer have successfully leveraged Numetrics tools to provide accurate, realistic IC project schedule estimates, identify unrealistic targets and plans, reduce schedule slip, and drive towards higher profitability. IC Project Planner effectively performs top-down risk analysis for each project and identifies unrealistic project plans so that corrective actions can be taken early to avoid late-stage disappointments.

At the portfolio level, MultiProject Pipeliner enables Messmer's management to view requirements for an entire IC development pipeline and compare them to available resources.