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SoC schedules: slip slidin' away

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(03/21/2008 2:55 AM EDT)

URL: <http://www.eetimes.com/showArticle.jhtml?articleID=206905136>

No prudent [chip](#) company would admit as much to customers, but the unspoken truth in today's complex world of system-on-chip (SoC) design is that most ICs will neither be developed nor delivered on time.

In fact, 89 percent of IC development projects miss their deadlines, according to Ron Collett, president and CEO at Numetrics Management Systems.

Consulting firm Accenture reports a similar trend, citing a range of schedule delays from as little as 3 percent to as much as 30 percent in IC development. If the IC in question is a lead, first-generation product--that is, a new chip requiring a new design--it will typically [register](#) an additional 15 to 30 percent delay in the design schedule, compared with a less-complex second, third, fourth or fifth spin of an existing product, said Scott Grant, senior executive with Accenture's Semiconductor Business Practice.

No customer would knowingly tolerate such delays. Nor could a reputable chip manufacturer intentionally budget such chronic overruns, especially with the cost of IC development skyrocketing. Schedule slips in IC development often result in a semiconductor company's missing an entire product cycle, losing prized design [wins](#) and triggering dangerous financial reverses.

EE Times has learned that Numetrics today will unveil enterprise resource planning (ERP) [software](#) tools designed to calculate chip design complexity, quantify scheduled risk, and estimate schedules and staffing requirements. While conventional [ERP](#) tools from Oracle, [SAP](#) or Siebel are used in managing sales, manufacturing, and general and administrative functions in an enterprise, none have existed thus far for semiconductor R&D organizations.

Numetrics has signed a multimillion-dollar, multiyear corporatewide agreement with NXP Semiconductors for its ERP offering. Numetrics claims that "six of the top 10" chip companies are already using Numetrics tools.

How bad is it?

A survey conducted last year by Embedded Systems Design, a sister publication of EE Times, found that the average embedded (not IC) development project comes in 4.1 months late. Numetrics' data shows that schedule slips for IC development vary, but they average 44 percent.

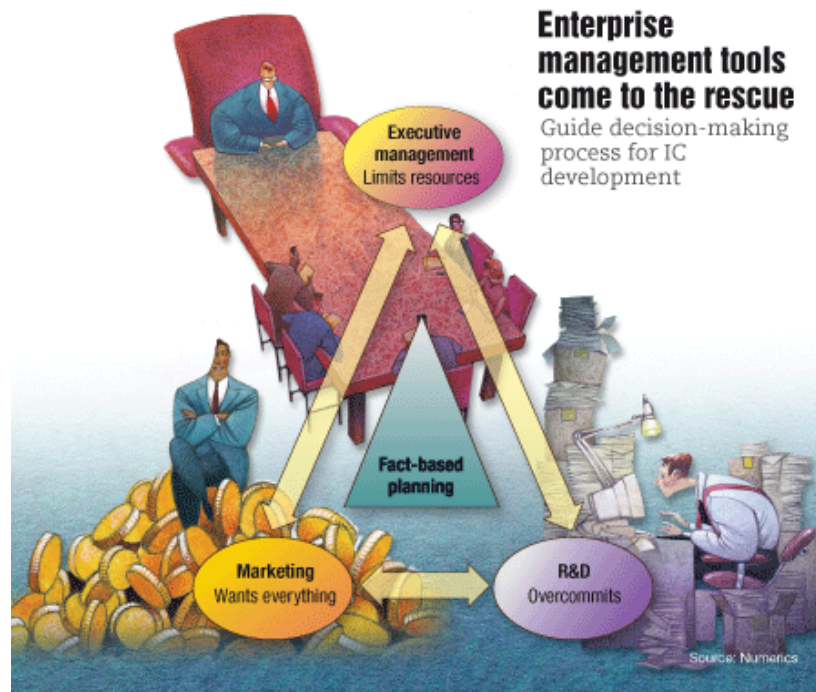
The reasons managers and designers cite for such delays range from "the intellectual property [core] was late" and "EDA tools are inadequate" to "a key manager left the organization" and "specs have changed." Collett calls them "the usual suspects" of excuses.

But the crux of the issue is unpredictability.

"You can't predict how challenging new functional-unit blocks [in a chip] will be and how complex the integration will be," said Accenture's Grant. "In many of these first-generation products, we have no way, even with historical data, to gauge what the newness factor is."

Taming that unpredictability is where Numetrics hopes to cash in.

Instead of dealing with a variety of individual causes for delays, Numerics' ERP software aims to look at the big picture. Collett developed the tool suite by leveraging the huge [database](#) the company has amassed since 2000 in the course of offering chip vendors services such as benchmarking IC development projects and measuring productivity against competitors.



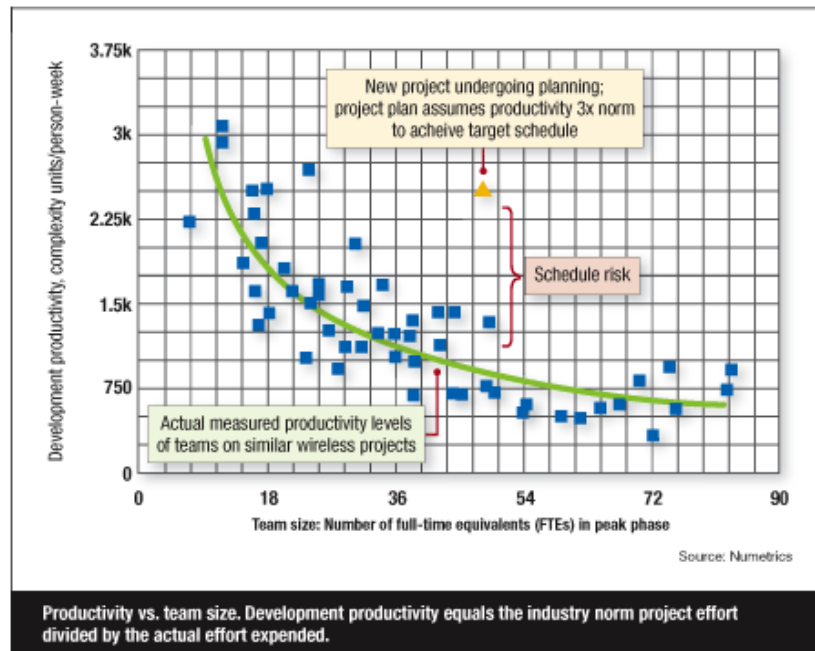
Collett believes IC development can be modeled as "a stochastic process," if adequate statistical data is available.

Variables introduced in such a process include the technical effects of shrinking die size and yields, a semiconductor R&D team's historical capabilities and tooling, and the impact of ever-expanding development teams that are often geographically far-flung. By pinning down such variables, "we can bring randomness into the model," Collett explained.

Expensive delays

Long delays are common in IC development, even among experienced chip vendors with ample engineering resources. For a high-profile example, one need look no further than an erstwhile Internet [Protocol](#) TV chip development partnership launched in 2004 between Microsoft Corp. and STMicroelectronics.

In looking for an innovative one-chip [multimedia processor](#) as a single hardware [platform](#) on which to develop its IPTV software, Microsoft settled on ST as its primary silicon vendor. But by November 2004, when Microsoft nabbed a \$400 million [IPTV](#) deal from AT&T (then SBC Communications), ST was experiencing a substantial delay in its promised IC development.



Within weeks, ST lost Microsoft's confidence. It was unseated by Sigma Design, which in early 2005 became Microsoft's primary prototype partner--a failure that cost ST dearly. Today, Sigma Design has a 100 percent lock on Microsoft's growing IPTV design sockets.

Thomas Wille, senior director of innovation and technology in business line identification at NXP Semiconductors, acknowledged that around the same time, his group was also "having trouble in getting products out." In 2004, the average product delay was as high as 40 to 50 percent. For the identification group, with an 80 percent market share in government projects such as national ID cards and electronic passports, this across-the-board slippage was unacceptable.

When asked why such slippage happens, Wille said, "First, we tend to underestimate the complexity of a chip-- especially when it is a brand-new product. [Second,] we tend to understaff the project." Particularly if the project runs more than one year, a "resource dilution" begins to take place, he said. "As the project gets prolonged, things happen here and there, people get distracted, they are pulled into different projects to help out others."

Indeed, most semiconductor R&D teams handle multiple IC development projects. "There is usually a portfolio of projects to manage in parallel," said Benoît Calimez, program manager for business line car entertainment solutions at NXP. Taking on a new project is hard enough, he said, but simultaneously sustaining products that are supposed to phase out but are still hanging fire further complicates project management.

Most chip companies tend to determine the schedule and resource requirements of a new IC project essentially by hunch. "We relied upon experts within the project or sometimes brought in experts from other projects at NXP who were regarded for their competence," said Calimez.

But in complex chip development, aligning the expectations of executive management, marketing and chip architects in the R&D organization is one of the hardest things for an organization to pull off. While the marketing department tends to want everything, executive management often limits resources and the R&D team ends up overcommitting.

Numetrics believes its ERP tools will help by offering fact-based information. "We'd like to think our tools are not only a friend of engineering teams, but also a friend of executive teams," Collett said.

The advantage of using Numetrics tools, said NXP's Calimez, is that "you can mix the quantitative data from Numetrics with the internal system's qualitative judgment."

After applying Numetrics' tools to nearly all of his group's projects, Wille said, "we improved predictability by 90 percent per year. Further, we made a 64 percent reduction in cycle time." Calimez noted that his group would not approve any project concept without first benchmarking the initial plans with an early project estimate from Numetrics.

Next step

Numetrics, of course, is not alone in analyzing delays and pioneering improvements in the various tools chip makers use. Another company tackling the problem is Silistix Inc. (San Jose, Calif.). David Lautzenheiser, vice president of marketing at Silistix, attributed chip development delays to "the move from single-function design to systems that require an altogether new approach than has historically been employed." The company is working to solve that problem.

Ken Lowe, vice president of strategic marketing at Sigma Design, pointed out that chip companies are under increasing pressure to get products out quickly. Today's new chips typically run much faster than earlier ICs, while chip geometry is getting ever smaller, he said. The company's SMP8634 chip used for IPTV set-top boxes and Blu-ray player/ recorders already has 4.5 million gates with 4 Mbits of memory. The next-generation chip consists of 7 million gates.

Accenture's Grant offered a few other reasons for schedule delays. Throughout the design life cycle, chip design requirements tend to be managed inconsistently, he said. There are "challenges with integrating chip design/product road maps, in tracking the overall bill-of-materials costs, and in storing and leveraging product data," said Grant.

Ultimately, Grant said, "The key question is: how do you connect, integrate the three layers of ERP, product life cycle management [PLM] and EDA tools?" ERP tools don't always talk to the other two. "Groups who are making progress with this are dealing with this challenge from a data perspective, such as product data," he said. "The aim is to get PLM connecting into the overall ERP tool."

Today, Numetrics' ERP tools target IC hardware design, but not software that runs on the ICs. That could turn out to be a major missing piece, especially as software complexity becomes a bigger factor in product development delays.

Numetrics indicated that an ERP tool for software development is on its way. NXP's Calimez said, "We are aggregating a database to help create software tools."

Numetrics' ERP software suite, called NMX-ERP 3.0, ranges from \$35,000 to \$95,000 per IC project, depending on each project's complexity and size.

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