

Faced with projects going late, chip designers are having to face up to doing less design themselves and buy in bigger lumps of circuitry, says **Chris Edwards**



out of time

CHIPMAKERS have a big problem. According to Numetrics Management Systems, most chip-design projects miss their deadlines. And it is because of reuse that it is happening – not because the intellectual property (IP) cores they buy but because teams choose to tinker with them.

Ron Collett, president and CEO of Numetrics, said at the IP07 conference late last year that the average chip-design project overruns by 44 per cent – adding almost six months to what is meant to be a year-long project. That is not good news when you consider that some consumer designs may be on the market for less than nine months, according to Scott

MacGregor, president of communications-silicon supplier Broadcom.

Collett's team collected data from a number of completed projects and found that 85 per cent of them missed their original schedule. The problem, he said, is that managers find it difficult to predict how long a project should take. "High schedule slip is equivalent to poor schedule predictability," he claims. "The core problem is that it is very difficult for design managers to predict design complexity and, especially, the impact of reuse."

The unexpected factor is the time needed to integrate IP cores from other sources, whether those cores come from inside the same company or from external

suppliers. Some of that pain is self-inflicted: teams are tinkering too much with the IP. But some just comes from the unanticipated cost of working with readymade logic blocks.

"Analyse it from the standpoint of what is the percentage of design-from-scratch effort versus the percentage of design reuse," says Collett.

Collett explained that even for complete reuse of a block with no modifications, some 8-10 per cent of the design effort that would be needed to implement a block of that size is required to integrate that block into a full chip. If you try to modify a block, the design effort needed for those changes and then to integrate the complete module shoots up.

"Once you get to the 50 per cent [redesign] point you get almost zero benefit from reuse. It almost pays to design it from scratch," Collett claims. "The range of significant benefit from reuse is in the 80 to 100 per cent range. That is less than intuitive to most IC development teams.

"The problem is that reuse expectations typically exceed reality. It is a core driver of schedule slip in the industry. [Project managers] think they are going to get a huge benefit and not expend nearly that level of effort. But, as soon as they start opening up and playing with the IP, the costs become significant," Collett says.

The rise in design effort when modifying IP can have a dramatic effect on schedule risk.

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Ron Collett, Numetrics



Collett presented the example of a six million-gate system-on-chip (SoC). If you add a further block to that of around 600,000 gates, the additional effort over a straight port to a new process technology should be around 24 per cent. However, the picture gets a lot worse if you spread those 600,000 gates across a number of blocks. Adding 10 per cent additional circuitry to a number of cores inside the chip instead of just adding a new block could easily double the engineering effort required, Collett claims.

"The total gate count is the same. But we get more than a doubling in effort simply by playing with all the blocks," Collett notes.

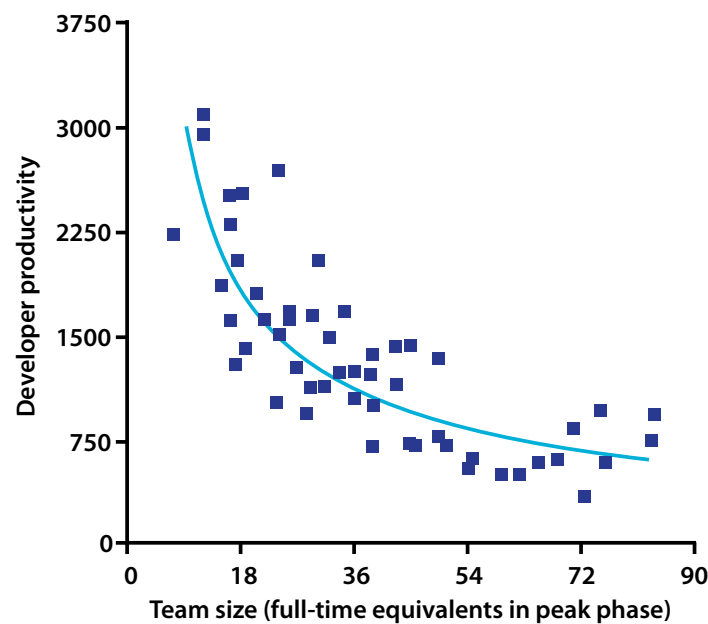
EXISTING MATERIALS

The answer, for some in the industry, is to be doing a lot less design and a lot more slotting together of pre-existing IP. But it will not be lots of little cores bought piecemeal in the way that most companies do it today. They will demand that their suppliers come up with complete subsystems, particularly for standard functions, with most of the legwork done already.

Gagan Gupta, senior director of product marketing at IP supplier ARC International, claims: "Consolidation in the IP industry is mimicking the convergence of functionality. You can't afford to get an audio engine from one person and the video from another. Users want a single provider to make sure the interoperability issues have been ironed out."

Alexander Haggenmiller, senior manager in Infineon Technologies computer-aided design department, agrees: "Last decade, we concentrated on the hardware [design] element. What is most interesting for us now is to have methodologies for integrating IP into the system."

In making predictions for his blog at Texas Instruments, Gene Frantz, principal fellow and business development manager for the digital signal processor maker, says: "IC designs will consist of smaller teams – five to



Small teams can be highly productive, as Numetrics has found from its surveys, but a lot depends on project complexity

ten designers – taking a shorter amount of time – six to 12 months – to do the hardware design. Reuse will be the norm.

"While I am at it, let me explain that there are two definitions of 'reuse'. [One is] I'll do such a good job on my design that everyone after me will use it. [The other is] I don't have time to reinvent the wheel, so I need to find something that is close enough to what I need to meet the schedule. Small design teams with short schedules will require us to use the latter definition. And, yes, there are companies already adopting this concept of reuse."

Haggenmiller sees it the same way: "SoC integration is a skill. With technology nodes that have smaller and smaller grids it becomes a key differentiator. The faster you can integrate the more it will be a differentiator for you."

Haggenmiller explained the problems that companies can run into when trying to focus too much on the minutiae of individual IP cores: "When it came to USB, we had five different versions of the same IP block. That is not reuse. But the situation has improved. We adapted our interconnectivity

system to a more structured architecture. The internal architecture of our chips is more flexible that it was ten years ago."

Haydn Povey, senior product marketing manager at ARM, warns that the trend to integration is not all one way: "The industry is looking for more integrated and complete solutions. But you have to balance that against the need to differentiate."

Povey pointed out that a small specialist supplier can often come up with something more innovative than a larger player trying to sell a function as part of a larger package.

For Jim Tully, chief of semiconductor research at analyst firm Gartner, the trend to use larger subsystems could see a shift in the balance of power in the IP industry. "We would also expect to see a growing interest in bigger IP blocks integrated together with software and offered as a total subsystem. We see interest from the processor vendors in that kind of thing. But it is really the design services companies, the design houses, who will capture most of that emerging sector," Tully forecasts. ■

delayed projects



TIME SLIPS BY

One surprising aspect of the research into chip-design schedules performed by Numetrics Management Systems is that the proportion of projects that go late has remained more or less static for ten years. That is despite the logic density of those chips increasing roughly ten-fold in that time.

The explanation for the lack of movement may come from the different attitude that the chipmakers now have to delayed projects compared to 1998.

"The numbers haven't changed but what has changed is that, in the old days, projects would go on in perpetuity. They would not get killed. The management then were very reluctant to kill off projects: there was a lot more margin in terms of time to market," Collett says. "Now, if those projects go late, they are far more likely to get killed, because the market window has disappeared. In our research, we don't count killed projects: we count only those that make it to production."

Another change is that companies have, on average, brought the design cycle time down even though the chips are far more complex. The average project used to take more than 120 weeks. Now the cycle time is down to around 80 weeks, Collett claims. But this is another area that chipmakers may start to look closely at: the increased capacity is partly down to ballooning team sizes. Since 2000, the average number of people on a project has doubled, he said, from 7.5 engineers to 13. And some teams number as many as 300, he notes.