Company Backgrounder

Starting a new complex IC design project is risky business. The stakes have never been higher-development costs will soar into the millions, the project will consume valuable engineers for perhaps 18 months or more, revenue from volume shipments remains years in the future, and the market window is narrow. A misjudgment in the schedule or staffing plan can be disastrous, especially in today's ultra competitive environment. There is little margin for error. How confident are you in your project plan? How sure are you that the project is staffed adequately to implement the target feature set in the required development time? Today, 85% of all IC projects miss their target schedule, with an average over-run of 44%.

What if you could...

- Quickly generate reliable schedule and staffing estimates for your project plan based on an accurate, quantitative assessment of your chip's design complexity?
- Quantitatively analyze and validate with high confidence your project schedule, staffing levels and other key assumptions in your plan?
- Instantaneously access an Industry Database of over 1,200 benchmarked IC projects whose design complexities have been normalized to enable calibration of your project plan against industry norms?
- Normalize the complexity of your past designs to better predict the staffing and schedule of your next project?
- Get an early-warning of schedule slip using proven tools and methods, to help avert scheduling disasters or over commitments before they happened?

Numetrics gives you precisely the capability to do all that. Based on sophisticated algorithms and statistical models calibrated with the most comprehensive database in the industry, Numetrics' NMX-ERP™ software is an invaluable asset to any semiconductor organization.

Numetrics' Mission:

Numetrics equips engineering and program managers with tools that deliver an accurate and quantitative perspective on the schedule and staffing decisions they are about to make. Starting with an estimate of the design's complexity, the NMX-ERP software tools approach the problem by modeling the development cycle as a stochastic, or random, process. From there, the tools perform three fundamental tasks:

1. Expose inherent risk in schedule and staffing assumptions by benchmarking your project plan's assumptions against a database of completed projects whose complexity has been normalized for accurate comparison to your particular design.
2. Allow you to do "fact-based" planning, which complements intuition based on prior project experiences
3. Perform "what if" project plan simulation, enabling managers to generate a range of different scenarios based on alternative IC product feature sets, staffing constraints and schedule targets.

The Bottom Line: Numetrics' software and services improve schedule predictability, which means less schedule slip, and at the same time, managers tap into the Industry Database to ensure that schedule targets are highly competitive. Projects finish on-time, within budget and boast competitive cycle times.

Numetrics' Approach:

How is it possible that Numetrics tools can accurately quantify risk, calculate design complexity and reliably estimate both project duration and staffing requirements? The answer lies in Numetrics' competitive advantage: The company spent years compiling a wealth of data by benchmarking over 1,200 production IC projects from over 35 semiconductor companies, examples of which are shown below. This data provides the foundation for developing powerful, empirically calibrated, estimation models.

Numetrics' Industry Database is the only database of its kind in the world and was compiled in connection with the company's benchmarking consulting practice. The

Database and consulting practice continue to offer semiconductor organizations a fast and reliable vehicle for determining how their chip development performance compares to the industry. Numetrics has benchmarked numerous projects in myriad categories, including wireless and wired communications, computing and peripherals, entertainment, industrial, and transportation. In fact, there over 20 different application segments, giving users unmatched capability to analyze project performance metrics of specific kinds of chips; supported design styles include SoC, RF and analog, mixed-signal design, ASICs, ASSPs, and advanced processors.

How we collect data

Core Competency. Data collection efficiency is a core competency of Numetrics that has been built into the NMX-ERP software. Based on years of benchmarking chip projects and applying its project planning and schedule risk analysis tools, Numetrics has determined which data is most important to capture. Furthermore, the NMX-ERP tools apply a methodology that allows users to successively and incrementally enter data, enabling them to generate reliable results but spend minimal effort entering data.

The data entered into the software includes technical information describing the chip, and schedule and staffing data that characterizes the project. Users can optionally capture any additional data they wish, to conduct further in-depth root cause analysis and performance base-lining for future project planning and risk analysis.

Project Planning & Execution Phases. During the very early stages of project planning, any fields left unpopulated are automatically filled with temporary values using industry norm data. Users update and revise entries as they gain more visibility into the design's specs and requirements, which further improves the quality of results. Initial schedule and staffing estimates can typically be generated with less than one hour of effort. Incremental updates during the planning and execution phases take minutes.

Project Closure. Upon the conclusion of the project, the final project data is captured and stored for future reference. The data can be automatically extracted from the user's internal EDA and ERP systems or entered manually. For manual entry, users typically spend four to six hours collecting the relevant data and another few hours to enter it into the system. This small time investment creates a baseline and knowledge base that enables the IC Project Planner software to rapidly generate reliable schedule & staffing estimates and measure schedule risk on future projects.

Protecting Confidentiality. Prior to including the project's performance metrics in the Industry Database, all confidential information is stripped from the project, including the company and project name, and any characteristics that would leave a "signature." Upon Numetrics' certification of data quality, and only upon the customer's approval and authorization, the project is added to the Database. Numetrics' professional services organization carefully scrutinizes each project's data before registering it in the Database. Numetrics maintains the customer's data in perpetuity, which means it's always accessible to that customer for use as a reference in future project planning and benchmarking. Naturally, Numetrics executes firm confidentiality agreements with all of its customers.

Numetrics' Capabilities:

Semiconductor organizations are accustomed to doing so-called "bottom-up" project planning. **Bottom-up** project planning itemizes tasks and orders them in time, either in parallel or sequentially. This inherently poses two challenges: trying to catalog every task and estimating the duration of each task. This may work satisfactorily for well-defined tasks and some phases of the project, but it tends to overlook the unexpected and under-represent the more variable periods of project activity. Bottom-up plans routinely underestimate and tend to be too optimistic.

Numetrics' **top-down approach** is inherently different. It models the IC development cycle as a stochastic process. A good example of the problem's stochastic nature is the additional time and effort triggered by unanticipated spec changes, library characterization and manufacturing process flaws, EDA software bugs, IP quality levels, logic design errors and other unpredictable events. All projects have unpredictable things happen to them, but treating the development cycle as a stochastic process and therefore modeling its randomness, is the cornerstone for achieving good schedule predictability.

Although it's impossible to know for sure which random events will occur or their individual impact, it is a foregone conclusion that a certain number will happen on almost every project and cause schedule slip. The modeling challenge is similar to modeling manufacturing yield-process manufacturing specialists compute and plot the probability of a random defect on a die of a certain size, even though neither the particular defect nor its occurrence on a specific wafer or die is known. However, one

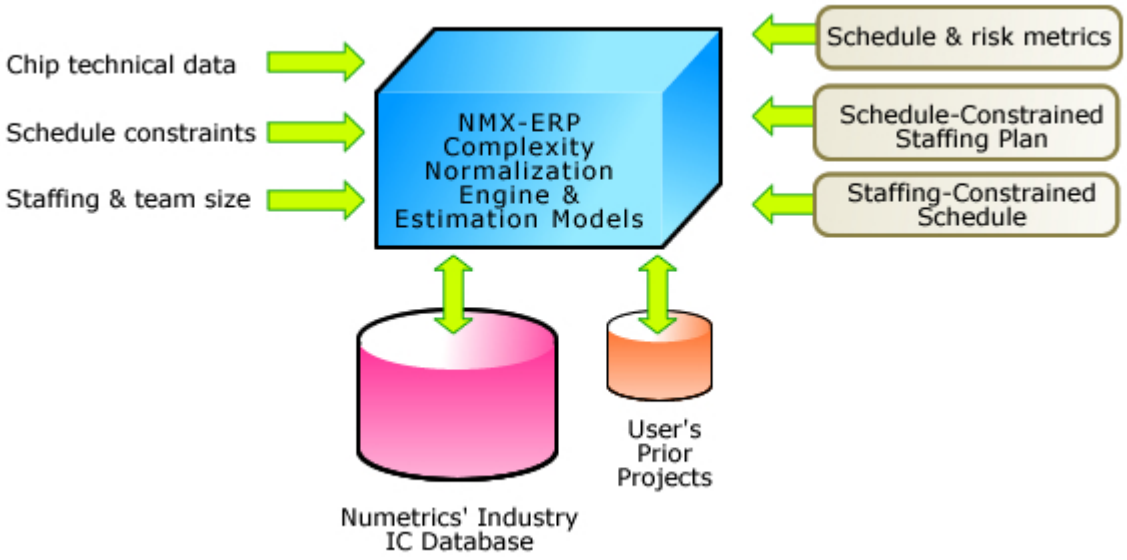
of the key things known is die size, and from this and other statistical data, process experts can accurately predict the number of good vs. bad die on a wafer.

Modeling Engineering Development as a Stochastic Process

Engineering managers can use similar analyses to estimate project effort. What's been missing until now are models calibrated with a sufficient amount of statistical data. For example, if engineering managers could determine the industry norm effort for the particular chip undergoing planning, they would have an excellent starting point for generating a more reliable staffing plan and schedule. Moreover, with the right models, a manager could then adjust the industry norm estimate to reflect the specifics of his or her particular project and team. This could be achieved with a simple knob that the manager uses to modulate team efficiency relative to industry norm. The amount of adjustment is based on the manager's knowledge of the development team and a few benchmarks of prior performance. This would yield a more precise estimate of the effort that particular team will need to expend on the project.

By generating a plan based on a precise calculation of the chip's complexity expressed as industry norm project effort, which is a calculation of the effort that the average team in the industry would expend on implementing that particular chip spec, and then modulating that effort with a probability density function of execution performance derived from hundreds of finished projects, the engineering manager has a statistically sound estimate of the cycle time and staffing requirements.

This type of estimate is statistically centered in the *envelope of reality*, defined by the execution performance achieved on prior projects having similar characteristics. Numetrics' top-down approach can be reliably applied earlier in the process than bottom-up planning, and with little effort, to help guide product direction and make better choices.



The Industry Database calibrates Numetrics' proprietary IC design complexity model and is the foundation of the NMX-ERP software suite. The patented complexity calculation engine is unique in the industry. Leveraging the Database, the engine accurately estimates the amount of effort required to develop the IC, from concept to volume production. The complexity model is the kernel for Numetrics risk analysis and project planning tools, which have been applied to over 500 production IC projects in the industry.

Numetrics' History:

Numetrics has been in business since 2000. But the research for Numetrics started much earlier. It began over 10 years ago with a goal of creating a framework for normalizing complexity of IC projects from all corners of the design world and framing them into statistical models from which users could extract valuable information. Numetrics' software represents over 300 person-years of work that has been validated by the top semiconductor companies.

The company's founder and CEO, Ron Collett, served as a Director of EDA and Semiconductor Research at Dataquest, a Gartner Group company, where he had the opportunity to meet with and analyze scores of companies. Later, when he founded Collett International, he had the opportunity to consult with dozens of leading semiconductor companies and start the process of developing stochastic methods to model the IC development process. Numetrics' history is rich with insights on what makes project fail or succeed based on actual data. This unique path and founders'

unique experiences makes Numetrics a one of its kind company in the semiconductor industry.

Six of the top ten semiconductor companies in the industry now use Numetrics' "fact-based" planning software and services to generate estimates of chip complexity, schedule and staffing requirements, and get rigorous, quantitative schedule risk assessments of their project plans-before committing to design implementation. With Numetrics tools, they're warned early of unacceptably high schedule risk-during the planning phase, when there's time to take corrective action. Equally important, managers now have the tools to conclusively identify project plans that fall outside a defined risk range. Starting a new, complex IC project is indeed risky business-but *only* if the risk of missing schedule goes unmeasured. What is risky is not measuring risk.

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